

Features

- +3 dBm Output Level at 1984 MHz
- Channel Step Size : 50 kHz
- 2nd Harmonic : < -20 dBc
- Spurious Level : < -65 dBc
- Lock Time : < 30 ms
- 50 mA Current Consumption

Description

The plerow™ PLL synthesizer module was designed for use in wireless and wireline systems in a wide range of frequency from 50 MHz to 6 GHz. ASB's PLL provides exceptionally low spurious and phase noise performance with fast locking time and low current consumption. All products are available in a surface-mount type package.



Specifications

Parameter	Unit	Min.	Typical	Max.
Frequency Range	MHz	1945	1984	2023
Output Power	dBm	+1	+3	
Supply Voltage	V	4.75	5	5.25
Current Consumption	mA			50
Channel Step Size	kHz		50	
2 nd Harmonics	dBc			-20
Spurious Level	dBc			-65
Lock Time	ms		10	30
Reference Frequency	MHz		10	
Reference Input Level	dBm	-5		+5
Phase Noise (C / N)				
@ 1 kHz			-	-
@ 10 kHz	dBc/Hz		-100	-95
@ 100 kHz			-120	-115
Output Impedance	Ω		50	
Operating Temp. Range	°C	-30	25	80
Package Type & Size	mm	SMT, 15.3W×15.3L×3.2H		

1) Measurement conditions are as follows: T = 25°C, V_{CC} = 5 V, Freq. = 1984 MHz, 50 ohm system.

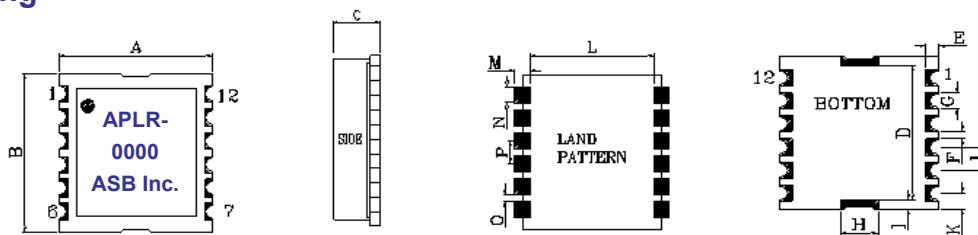
More Information

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Outline Drawing



Dimension (Tolerance ±0.2)															UNIT : mm	
Symbol	A	B	C	D	E	F	G	H	I	J	K	L	N	M	O	P
Size	15.3	15.3	3.20	13.90	1.30	0.51	1.52	6.0	0.80	2.03	2.58	12.7	1.52	2.40	0.51	2.03

Pin Out for PLL			
Pin No.	Application	Pin No.	Application
2	CLOCK	8	OSC IN
3	VCC (VCO)	9	VCC (PLL)
4	LOCK DETECT	10	DATA
5	RF OUT	11	ENABLE
All other Pins are Grounded			