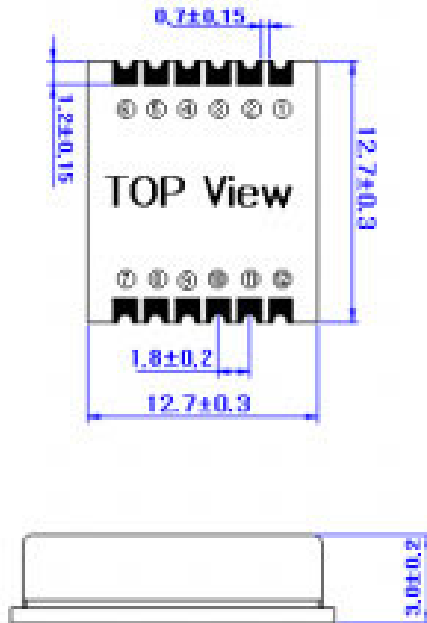
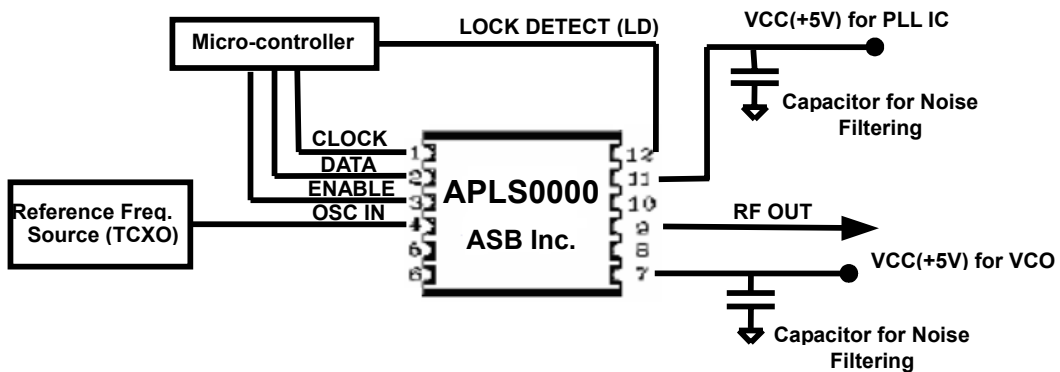


APLS0000 Type

Type	Dimension
Standard (PLL IC + VCO)	12.7 x 12.7 x 3

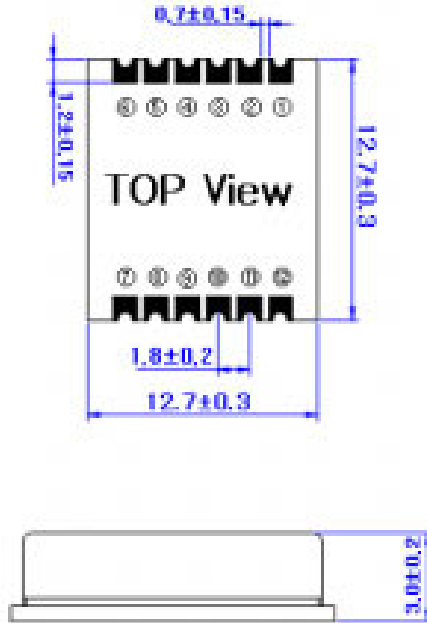


Pin Out for PLL			
Pin No.	Application	Pin No.	Application
1	CLOCK	7	VCC (VCO)
2	DATA	9	RF OUT
3	ENABLE	11	VCC (PLL)
4	OSC IN	12	LOCK DETECT
All other Pins are Grounded			

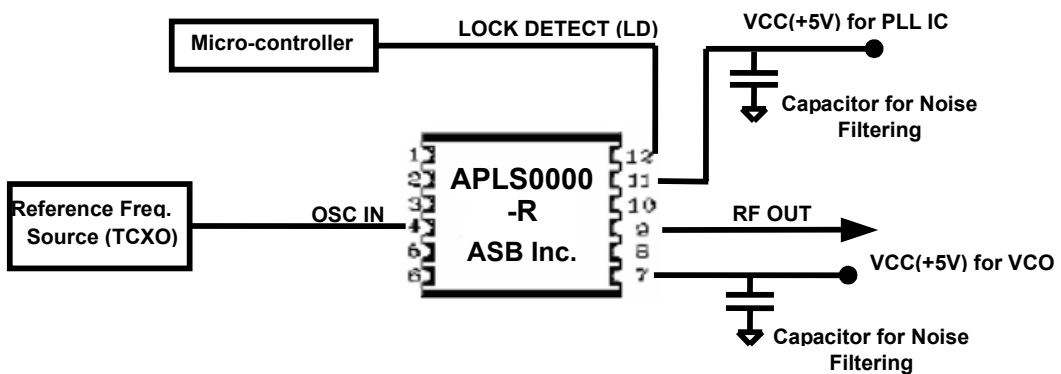


APLS0000-R Type

Type	Dimension
PLL IC + VCO + ROM	12.7 x 12.7 x 3

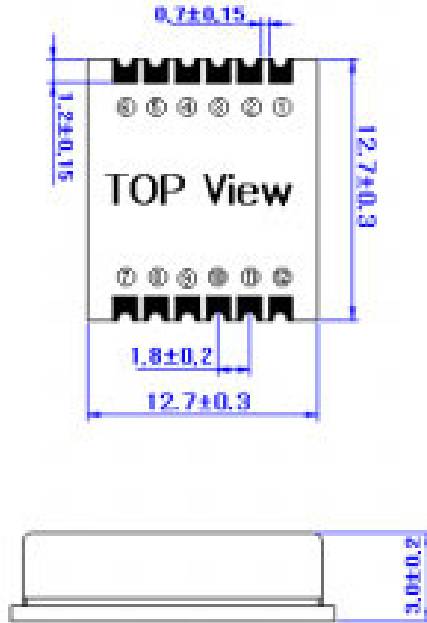


Pin Out for PLL			
Pin No.	Application	Pin No.	Application
1	GROUND	7	VCC (VCO)
2	GROUND	9	RF OUT
3	GROUND	11	VCC (PLL)
4	OSC IN	12	LOCK DETECT
All other Pins are Grounded / Internal ROM			

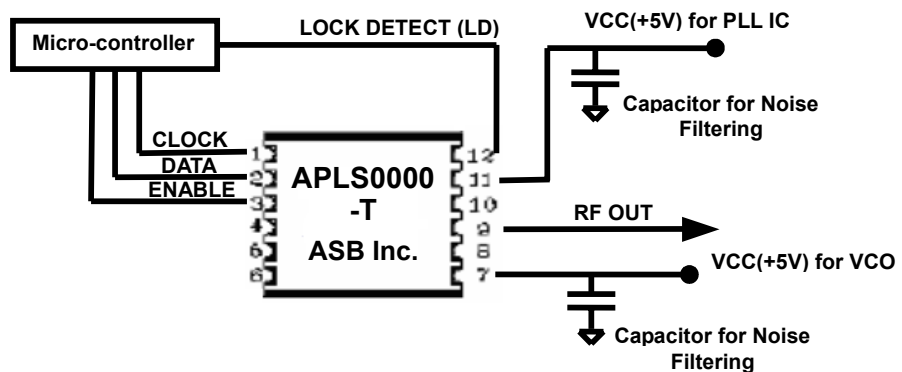


APLS0000-T Type

Type	Dimension
PLL IC + VCO + TCXO	12.7 x 12.7 x 3

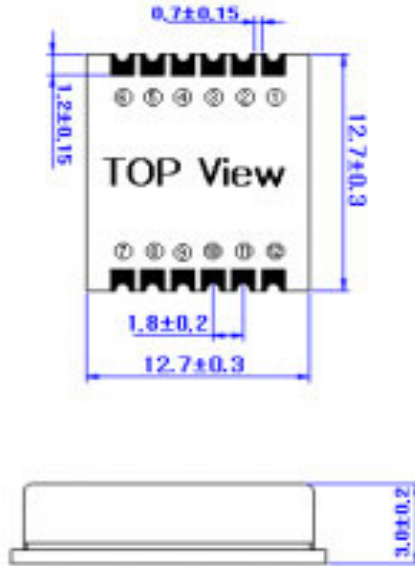


Pin Out for PLL			
Pin No.	Application	Pin No.	Application
1	CLOCK	7	VCC (VCO)
2	DATA	9	RF OUT
3	ENABLE	11	VCC (PLL)
4	GROUND	12	LOCK DETECT
All other Pins are Grounded / Internal TCXO			

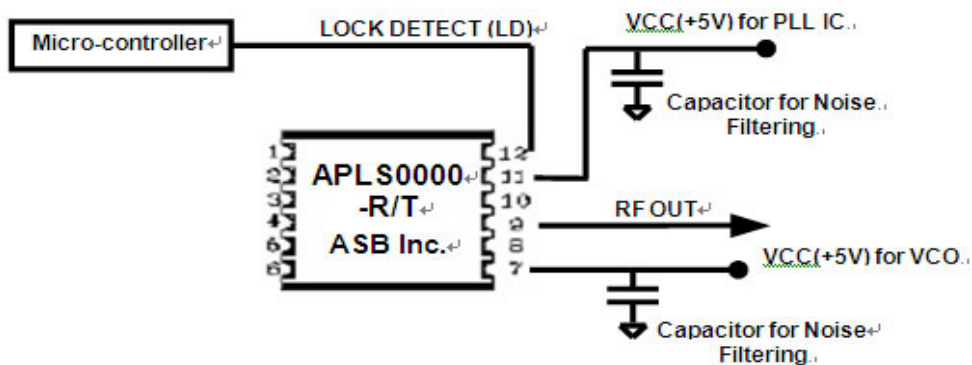


APLS0000-R/T Type

Type	Dimension
PLL IC + VCO + ROM + TCXO	12.7 x 12.7 x 3



Pin Out for PLL			
Pin No.	Application	Pin No.	Application
1	GROUND	7	VCC (VCO)
2	GROUND	9	RF OUT
3	GROUND	11	VCC (PLL)
4	GROUND	12	LOCK DETECT
All other Pins are Grounded / Internal TCXO and ROM			



Application Note

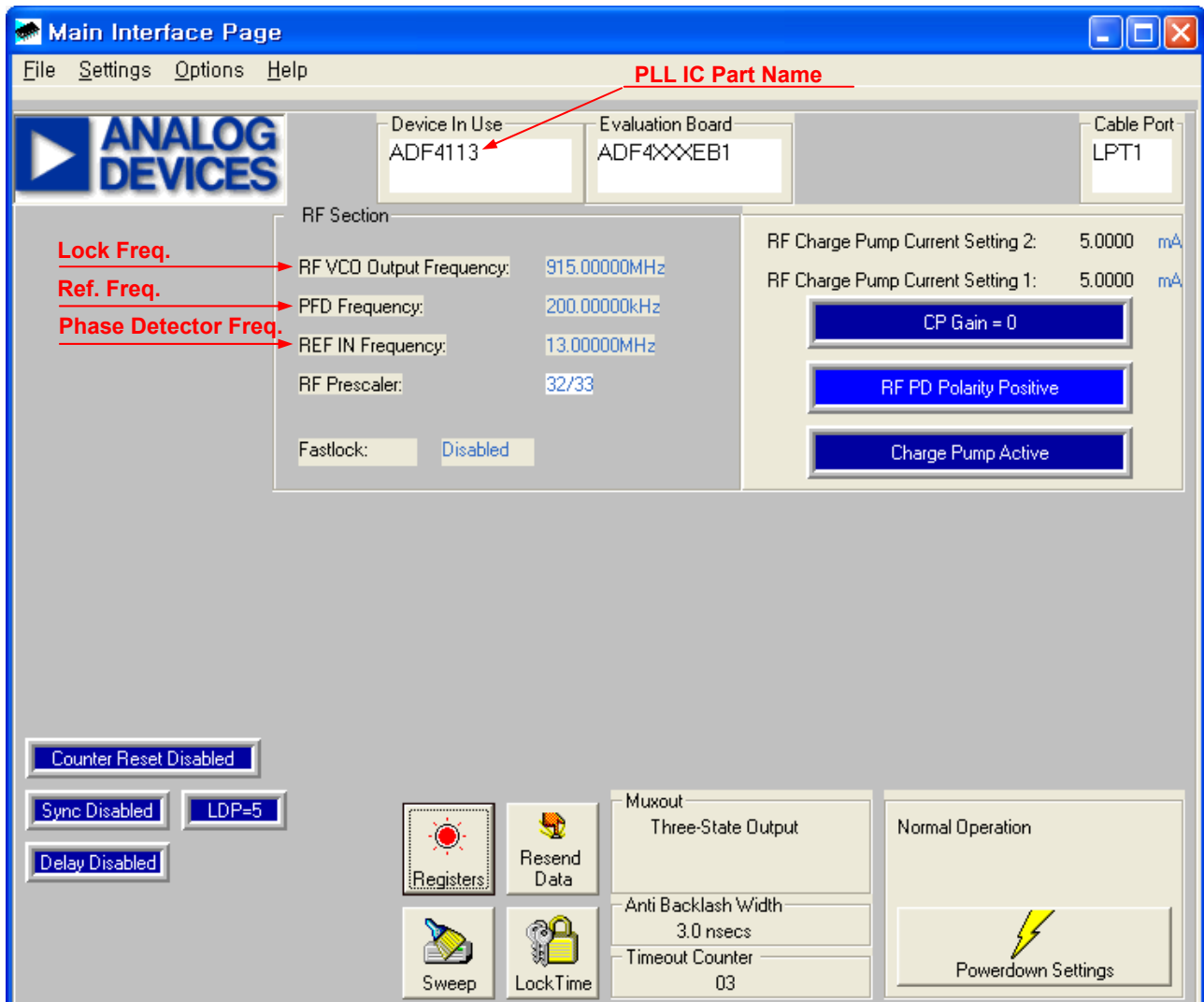
1) PLL IC : ADF4113 (Vendor : Analog Devices) or compatible chips

- Refer to the ADF4113 Datasheet to find how to control PLL.

- Download the PLL IC control program at the

[http://www.analog.com/en/rfif-components/pll-](http://www.analog.com/en/rfif-components/pll-synthesizersvcos/products/eb_PLL_download_software/fca.html)

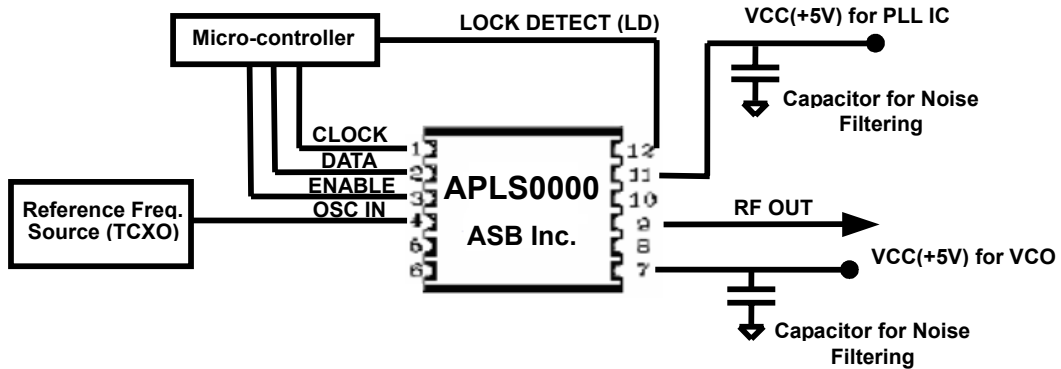
[synthesizersvcos/products/eb_PLL_download_software/fca.html](http://www.analog.com/en/rfif-components/pll-synthesizersvcos/products/eb_PLL_download_software/fca.html)



Main Interface Page <Example for APLS0915-T>

(Lock Freq.= 915MHz, Ref. Freq.=13MHz, Phase Detector Freq.= 200kHz)

2) Application circuit diagram



1. Capacitances for the noise filtering are selected upon the noise characteristics (frequency spectrum, power level) from the power supplies. From a few tens of μF to a few hundreds of μF is recommended.
2. For APLS0000-R(ROM built-in), the “CLOCK”, “DATA”, “ENABLE” pins are not necessary to be connected.
3. For APLS0000-T(TCXO built-in), the reference frequency source is not necessary to be connected
4. For APLS0000-R/T(ROM & TCXO built-in), the “CLOCK”, “DATA”, “ENABLE”, reference frequency source pins are not necessary to be connected.

3) Pin description

Pin Name	Description	Remarks
CLOCK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 21-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.	
DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs as the control bits. This input is a high impedance CMOS input.	
ENABLE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.	
LD	This multiplexer output allows either the lock detect (LD), the scaled RF, or the scaled reference frequency to be accessed externally.	

* Refer to ADF4113 datasheet for detail.