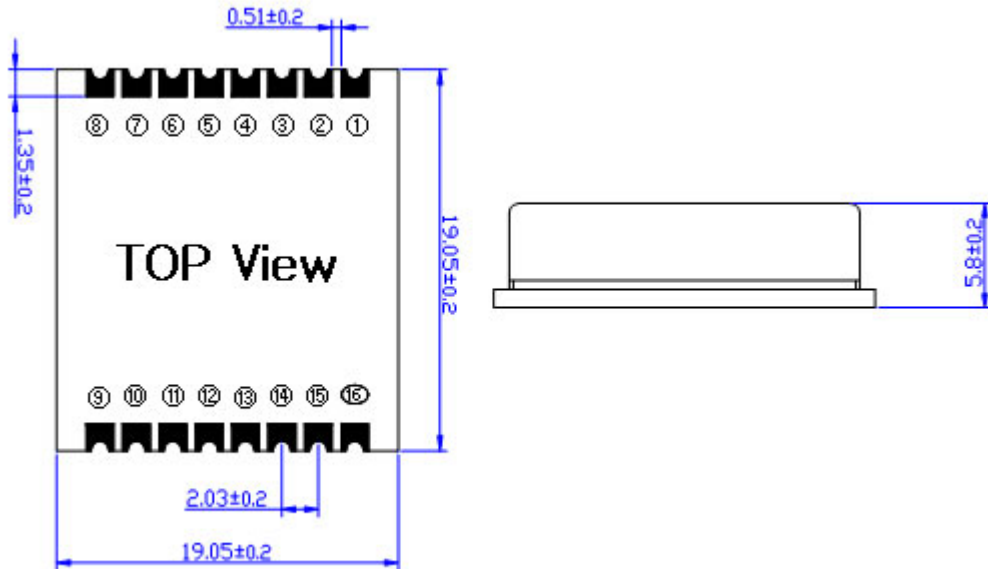
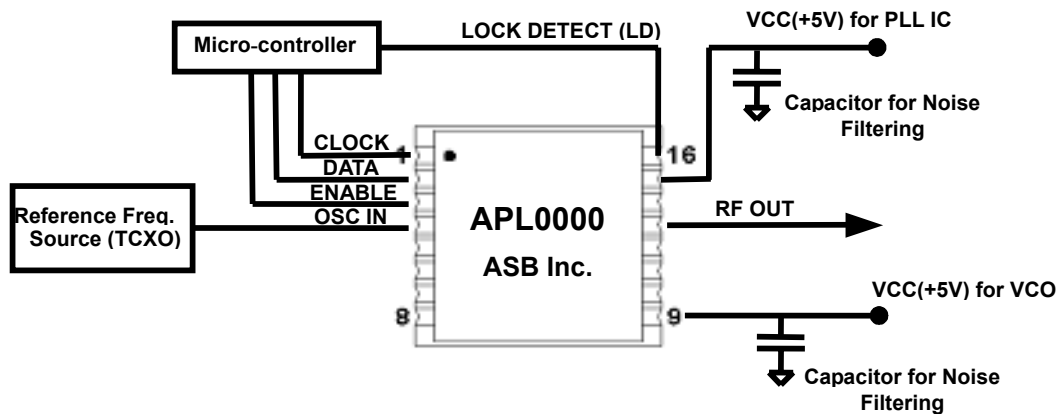


**APL0000 Type**

Type	Dimension
Standard (PLL IC + VCO)	19 x 19 x 5.8

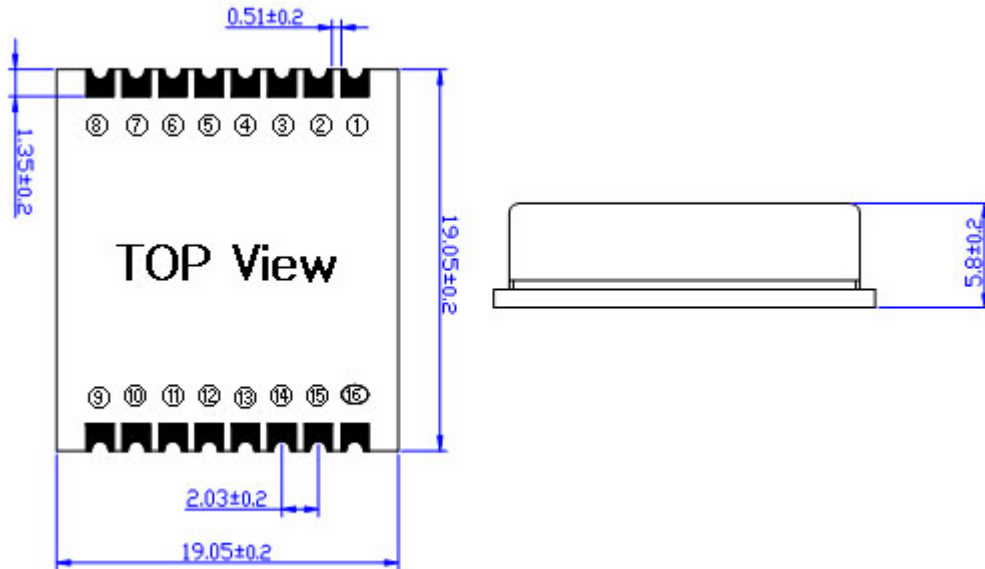


Pin Out for PLL			
Pin No.	Application	Pin No.	Application
1	CLOCK	9	VCC (VCO)
2	DATA	13	RF OUT
3	ENABLE	15	VCC (PLL)
4	OSC IN	16	LOCK DETECT
All other Pins are Grounded			

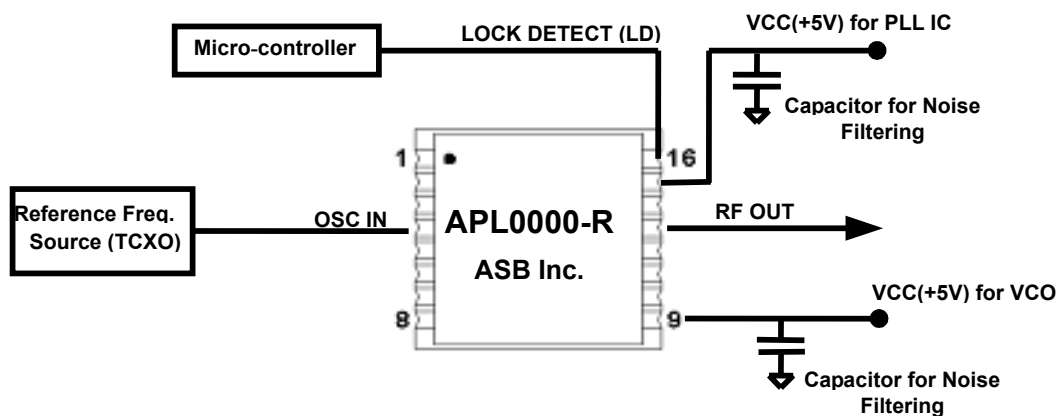


**APL0000-R Type**

Type	Dimension
PLL IC + VCO + ROM	19 x 19 x 5.8

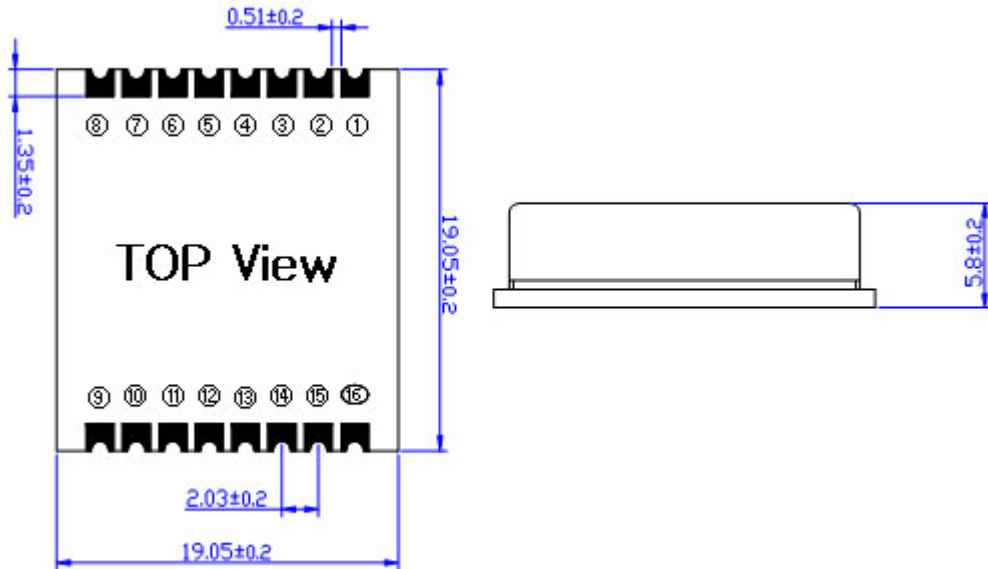


Pin Out for PLL			
Pin No.	Application	Pin No.	Application
1	GROUND	9	VCC (VCO)
2	GROUND	13	RF OUT
3	GROUND	15	VCC (PLL)
4	OSC IN	16	LOCK DETECT
All other Pins are Grounded / Internal ROM			

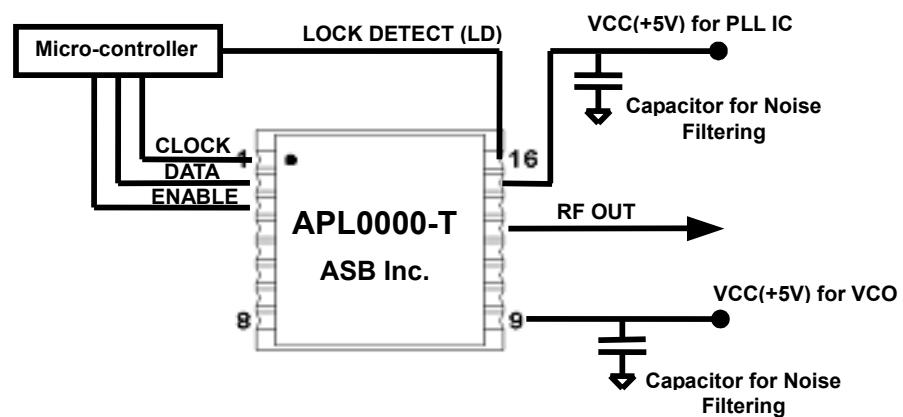


**APL0000-T Type**

Type	Dimension
PLL IC + VCO + TCXO	19 x 19 x 5.8

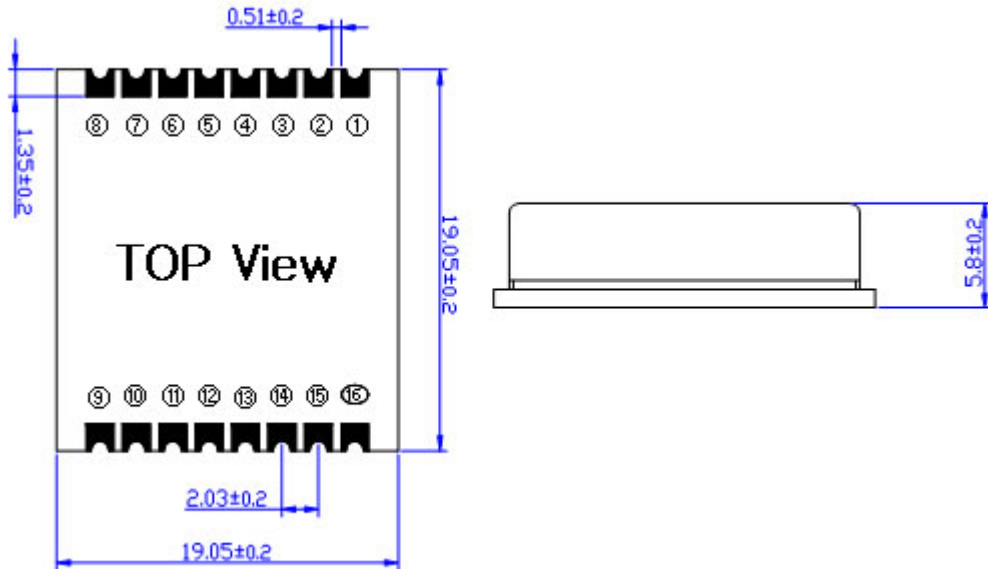


Pin Out for PLL			
Pin No.	Application	Pin No.	Application
1	CLOCK	9	VCC (VCO)
2	DATA	13	RF OUT
3	ENABLE	15	VCC (PLL)
4	GROUND	16	LOCK DETECT
All other Pins are Grounded / Internal TCXO			

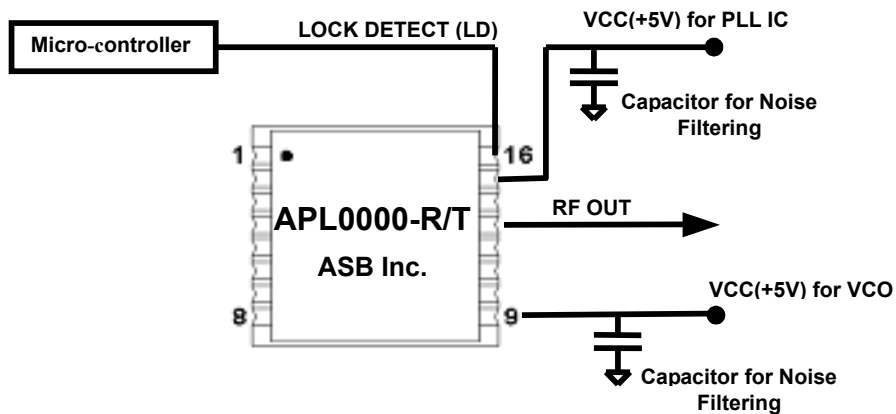


**APL0000-R/T Type**

Type	Dimension
PLL IC + VCO + ROM + TCXO	19 x 19 x 5.8



Pin Out for PLL			
Pin No.	Application	Pin No.	Application
1	GROUND	7	VCC (VCO)
2	GROUND	10	RF OUT
3	GROUND	11	VCC (PLL)
4	GROUND	12	LOCK DETECT
All other Pins are Grounded / Internal TCXO and ROM			



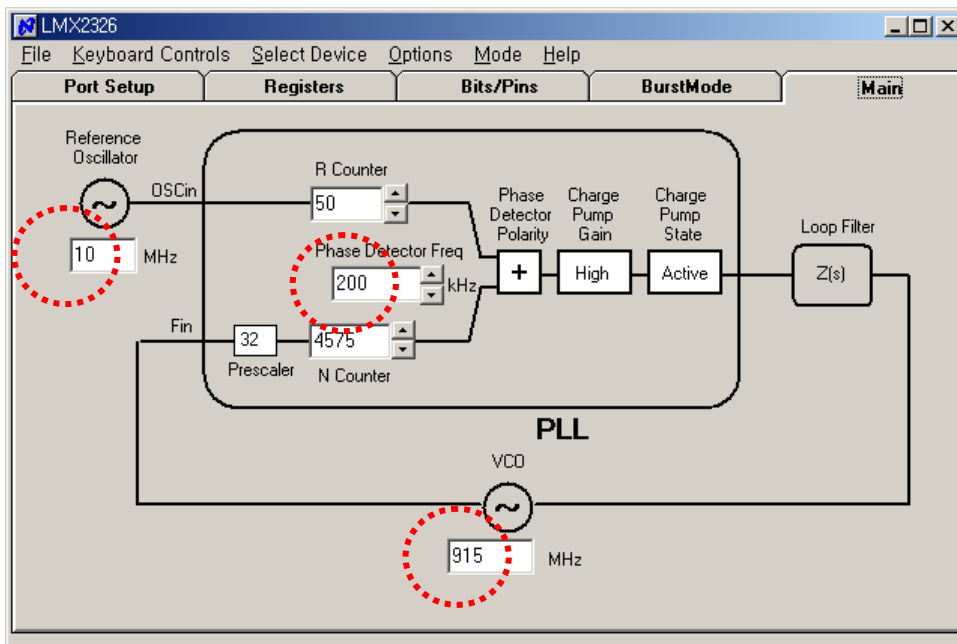
## Application Note

### 1) PLL IC : LMX2326 (Vendor : National Semiconductor) or compatible chips

- Refer to the LMX2326 Datasheet to find how to control PLL.

- Download the PLL IC control program at the

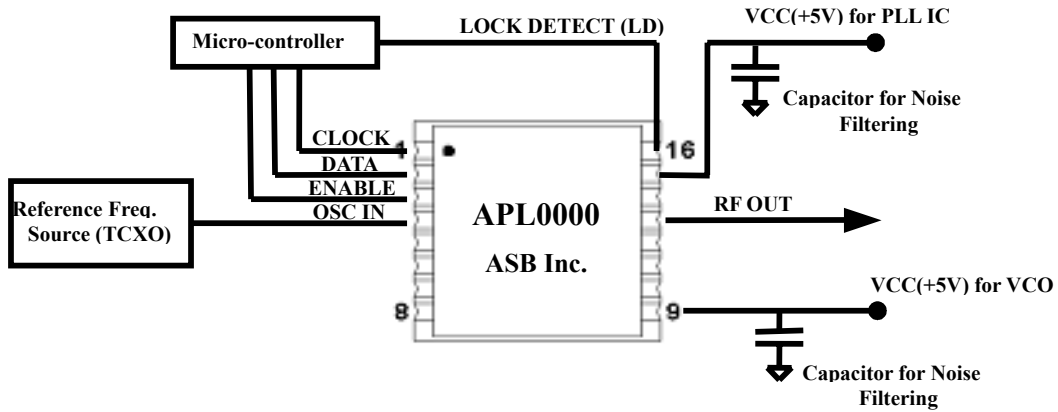
<http://webench.national.com/appinfo/wireless/0,1822,185,00.html>



#### Main Screen <Example for APL0915>

(Lock Freq.= 915MHz, Ref. Freq.=10MHz, Phase Detector Freq.= 200kHz)

## 2) Application circuit diagram



1. Capacitances for the noise filtering are selected upon the noise characteristics (frequency spectrum, power level) from the power supplies. From a few tens of  $\mu\text{F}$  to a few hundreds of  $\mu\text{F}$  is recommended.
2. For APL0000-R (ROM built-in), the "CLOCK", "DATA", "ENABLE" pins are not necessary to be connected.
3. For APL0000-T (TCXO built-in), the reference frequency source is not necessary to be connected.
4. For APL0000-R/T (ROM & TCXO built-in), the "CLOCK", "DATA", "ENABLE", reference frequency source pins are not necessary to be connected.

## 3) Pin description

Pin Name	Description	Remarks
CLOCK	High Impedance CMOS Clock Input. Data for the various counters is clocked in on the rising edge into the 21-bit shift register.	
DATA	Binary Serial Data Input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.	
ENABLE	Load Enable CMOS Input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 3 appropriate latches (control bit dependent).	
LD	Multiplexed Output of the RF Programmable or Reference Dividers and Lock Detect. CMOS output.	

\* Refer to LMX2326 datasheet for detail.

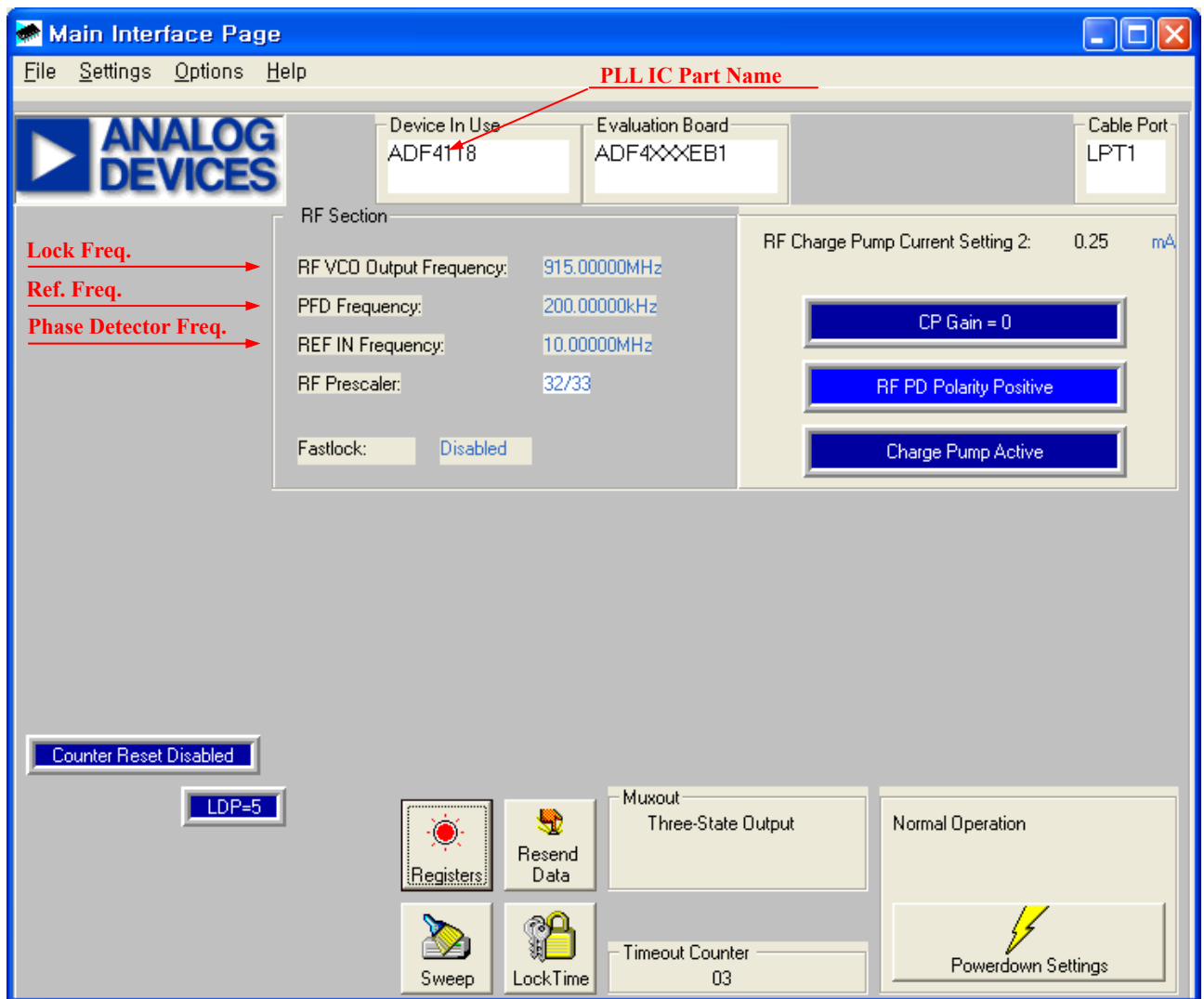
## Application Note

### 1) PLL IC : ADF4118 (Vendor : Analog Devices) or compatible chips

- Refer to the ADF4118 Datasheet to find how to control PLL.

- Download the PLL IC control program at the

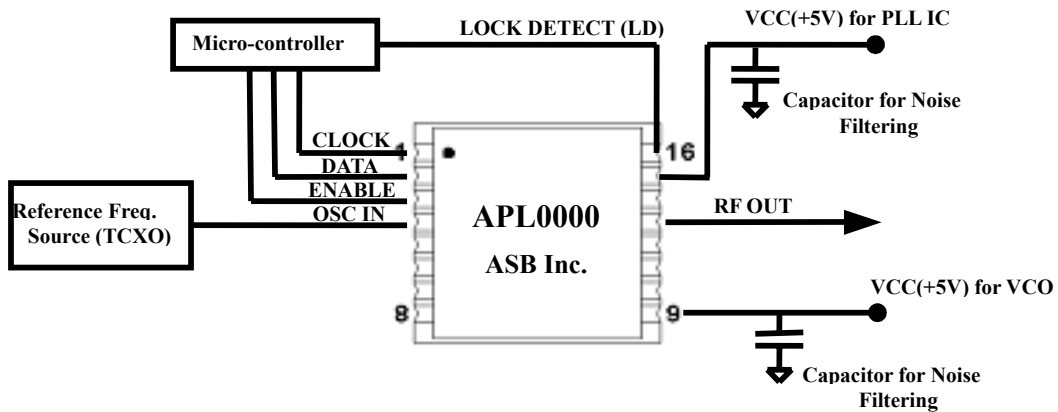
[http://www.analog.com/en/rfif-components/pll-synthesizersvcos/products/eb\\_PLL\\_download\\_software/fca.html](http://www.analog.com/en/rfif-components/pll-synthesizersvcos/products/eb_PLL_download_software/fca.html)



**Main Interface Page <Example for APL0915>**

(Lock Freq.= 915MHz, Ref. Freq.=10MHz, Phase Detector Freq.= 200kHz)

## 2) Application circuit diagram



1. Capacitances for the noise filtering are selected upon the noise characteristics (frequency spectrum, power level) from the power supplies. From a few tens of  $\mu\text{F}$  to a few hundreds of  $\mu\text{F}$  is recommended.
2. For APL0000-R (ROM built-in), the "CLOCK", "DATA", "ENABLE" pins are not necessary to be connected.
3. For APL0000-T (TCXO built-in), the reference frequency source is not necessary to be connected.
4. For APL0000-R/T (ROM & TCXO built-in), the "CLOCK", "DATA", "ENABLE", reference frequency source pins are not necessary to be connected.

## 3) Pin description

Pin Name	Description	Remarks
CLOCK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 21-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.	
DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs as the control bits. This input is a high impedance CMOS input.	
ENABLE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.	
LD	This multiplexer output allows either the lock detect (LD), the scaled RF, or the scaled reference frequency to be accessed externally.	

\* Refer to ADF4118 datasheet for detail.