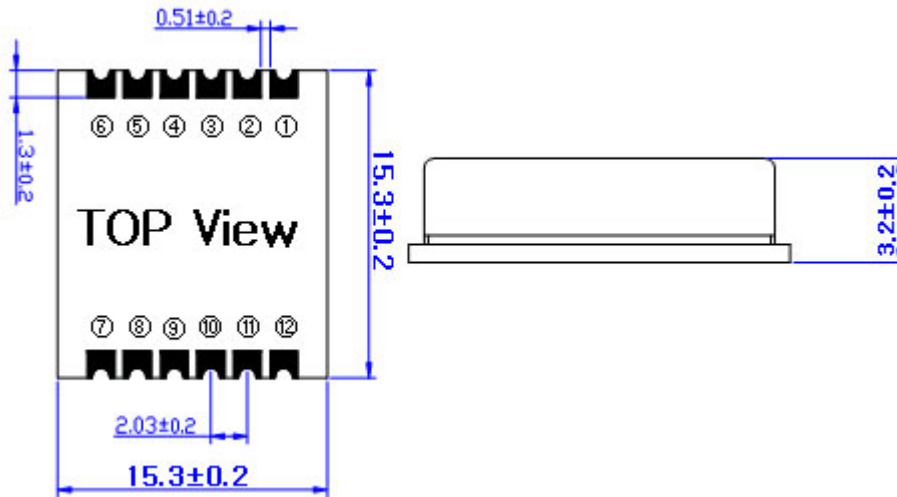
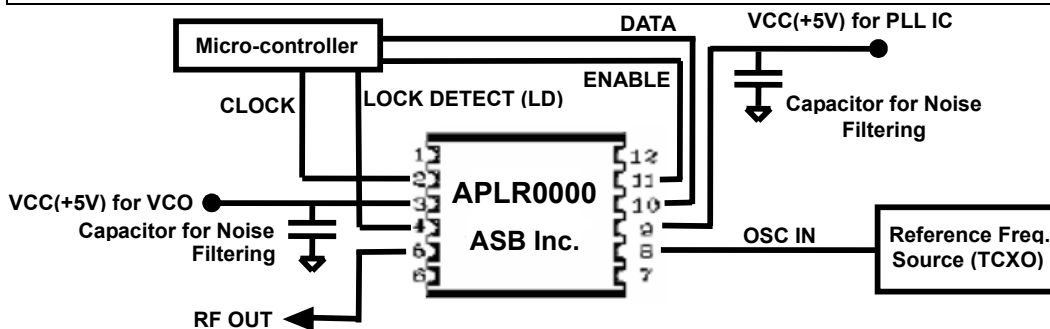


**APLR0000 Type**

Type	Dimension
Standard (PLL IC + VCO)	15.3 x 15.3 x 3.2



Pin Out for PLL			
Pin No.	Application	Pin No.	Application
1	GND	7	GND
2	CLOCK	8	OSC IN
3	VCC (VCO)	9	VCC (PLL)
4	LOCK DETECT	10	DATA
5	RF OUT	11	ENABLE
All other Pins are Grounded			

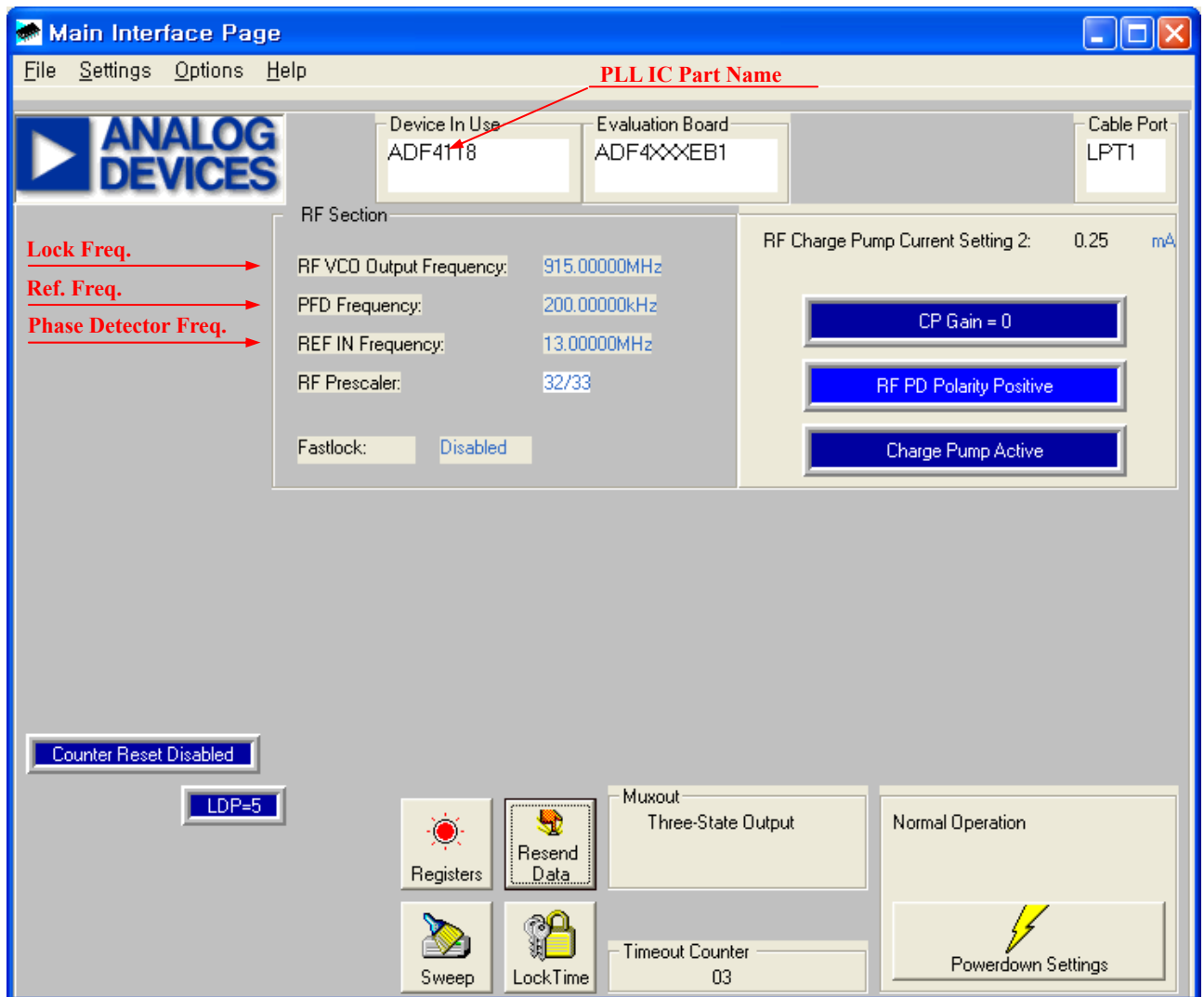


**Application Note**

**1) PLL IC : ADF4118 (Vendor : Analog Devices) or compatible chips**

- Refer to the ADF4118 Datasheet to find how to control PLL.
- Download the PLL IC control program at the

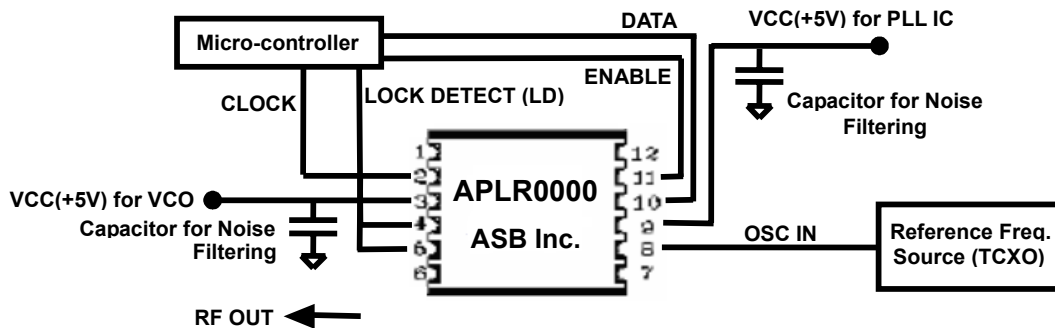
[http://www.analog.com/en/rfif-components/pll-synthesizersvcos/products/eb\\_PLL\\_download\\_software/fca.html](http://www.analog.com/en/rfif-components/pll-synthesizersvcos/products/eb_PLL_download_software/fca.html)



**Main Interface Page <Example for APLT0915-T>**

(Lock Freq.= 915MHz, Ref. Freq.=13MHz, Phase Detector Freq.= 200kHz)

**2) Application circuit diagram**



1. Capacitances for the noise filtering are selected upon the noise characteristics (frequency spectrum, power level) from the power supplies. From a few tens of  $\mu\text{F}$  to a few hundreds of  $\mu\text{F}$  is recommended.
2. For APLT0000-R(ROM built-in), the “CLOCK”, “DATA”, “ENABLE” pins are not necessary to be connected.
3. For APLT0000-T(TCXO built-in), the reference frequency source is not necessary to be connected
4. For APLT0000-R/T(ROM & TCXO built-in), the “CLOCK”, “DATA”, “ENABLE”, reference frequency source pins are not necessary to be connected.

**3) Pin description**

Pin Name	Description	Remarks
CLOCK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 21-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.	
DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs as the control bits. This input is a high impedance CMOS input.	
ENABLE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.	
LD	This multiplexer output allows either the lock detect (LD), the scaled RF, or the scaled reference frequency to be accessed externally.	

\* Refer to ADF4118 datasheet for detail.

5.